AMENDMENTS TO THE DRAWINGS

Please replace sheets 1-7 of the drawings with the replacement sheets 1-8 attached at the end of this paper.

REMARKS

This application has been reviewed in light of the Office Action mailed May 20, 2005. Reconsideration of this application in view of the below remarks is respectfully requested. Claims 1-38 are pending in the application with Claims 5-20, 25-29, 31 and 33-36 having been withdrawn. Of the presently elected claims, Claim 1 is in independent form. By the present amendment, Claim 1 has been amended and Claims 37 and 38 have been newly added. No new subject matter has been introduced by way of the present amendment.

I. Objection to the Drawings

The drawings have been objected to because of handwritten notations and text that is too small. After review of the drawings contained in the file wrapper, it appears that the drawing sheets had been reduced in size when scanned. This may have contributed to the small character size. However, in response to the Examiner's request, replacement sheets for FIGS. 1-8 have been submitted, by way of the present amendment.

II. Objection to Claims 1-4, 21-24, 30 and 32

Claims 1-4, 21-24, 30 and 32 have been objected to because of informalities. Specifically, the Examiner asserts that the phrase: "A test circuit..." recited by Claims 2-4, 21-24, 30 and 32 should be rephrased as: "The test circuit...", since Claims 2-4, 21-24, 30 and 32 are referring to the same test circuit introduced in Claim 1. In response, Claims 2-4, 21-24, 30 and 32 have been amended to comply with the Examiner's request.

Additionally, the Examiner requests the term: "therein" be rephrased to clarify the location of the scan path test circuit. In response, the preamble of Claim 1 has been amended to recite: "A test circuit for a semiconductor integrated circuit device for being put to a delay test

using a scan path test circuit incorporated on said semiconductor integrated circuit device for a scan path test..." (Emphasis added).

III. Rejection of Claims 22 and 32 Under 35 U.S.C. §112, Second Paragraph

Claims 22 and 32 have been rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter, which the applicant regards as the invention. Specifically, the Examiner asserts that the term "easily" recited in Claims 22 and 32, is a relative term since the specification does not provide a standard for ascertaining the requisite degree. In response, Claims 22 and 32 have been amended to recite: "...a frequency divider mounted on said test board, for dividing the frequency of said test clock into a lower frequency", thus rendering the rejection moot.

IV. Rejection of Claims 1 and 2 Under 35 U.S.C. §102(b)

Claims 1 and 2 have been rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 5,524,114 issued to Peng.

Peng discloses a scan path test circuit having a two-pulse generator for the delay test. In Peng, the coincidence of CTL 112 logic low, and leading edge clock pulses 316 and 312 at time 318 begins the scan-path test. Clock pulses 312 of SCK-1 222 are at a higher frequency (faster speed) than the TCK 110 clock pulses 316. The clock pulses 312 and 316 are phase locked in frequency and phase, therefore each clock pulse leading edge, when going from a logic low to a logic high, will occur at substantially the same time as is indicated by the number 318. (See: FIG. 2 and 3; and col. 7, lines 32-50).

Two clock pulses 310a and 310b are generated at the same time when TCK 110 is at logic high after CTL has gone to logic low. Therefore, in Peng, a falling edge of CTL 112, a rising edge of TCK 110 and two clock pulses 310a and 310b occur at almost the same time. However,

the falling edge of CTL 112 and rising edge of TCK 110 generates noise, which may influence the measurement of the delay test.

Contrastingly, Applicant's gate signal generator does not output a two-pulse clock signal immediately after the control pulse is input to a two-pulse generator, but rather generates the pulse after a fixed interval.

Referring to FIG. 3 and FIG. 4 to illustrate the above feature, when the control pulse is input to two-pulse generator 3, a given number of pulses of the test clock elapse before frequency divider 201 begins generating gate signal GT. Latch gate circuit 100 passes the test block only while the gate signal GT is at logic high, thus outputting a two-pulse clock signal for a delay test. (See: Applicant's page 9, lines 15-20). Therefore, Peng fails to anticipate having the gate signal generator generate a gate signal after a predetermined interval as measured from an input timing of a control signal, as recited in Applicant's independent Claim 1. Claim 2 depends from independent Claim 1 and thus recites all the limitations of that independent claim. Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claims 1 and 2 under 35 U.S.C. §102(b).

V. Rejection of Claims 3-4, 21-24, 30 and 32 Under 35 U.S.C. §103(a)

Claims 3-4, 21-24, 30 and 32 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentably obvious over Peng in view of U.S. Patent No. 5,794,175 issued to Conner. Claims 3-4, 21-24, 30 and 32 depend from independent Claim 1 and thus recite all the limitations of that independent claim.

While Conner discloses a printed circuit board (PCB) memory array board 210 having a plurality of sockets for burn-in quality testing, there is, however, no disclosure or suggestion of a delay test and two-pulse generator, wherein a gate signal generator generate a gate signal after a

predetermined interval as measured from an input timing of a control signal, as recited in Applicant's independent Claim 1.

Regarding the rejection of Claims 4 and 30, the Examiner asserts that frequency divider 210 of Peng is equivalent to the claimed frequency multiplying PLL circuit by citing that dividing a frequency by N is the equivalent of multiplying that same frequency by 1/N. However, while this is mathematically correct, the result is not equivalent since multiplying the frequency by 1/N will reduce the frequency. What is meant by "to multiply the frequency" as recited in the claim and supported throughout the specification is "to increase the frequency" by a given factor. Additionally, supporting circuitry would be necessary to allow an input of value N to produce a multiplied frequency output of (N*frequency) using a frequency divider 210, thus the frequency divider 210 and the frequency multiplying PLL cannot properly be equated.

Conner fails to overcome the above-identified deficiencies of Peng, and so Peng and Conner, taken alone or in any proper combination, fail to disclose or suggest the limitations recited in Applicant's Claim 1. Accordingly, for at least the reasons given above, Applicant respectfully requests withdrawal of the rejection with respect to Claims 3-4, 21-24, 30 and 32 under 35 U.S.C. §103(a) over Peng in view of Conner.

VI. New Claims 37 and 38

By way of the present amendment, Claims 37 and 38, reciting: "The test circuit according to claim 1, wherein said gate signal generator comprises a control circuit for adjusting a timing of said gate signal" and "The test circuit according to claim 37, wherein said control circuit counts said test clock for adjusting said timing of said gate signal" respectively, have been newly added. The limitations recited in these new claims are supported in FIG. 3 and on page 2, paragraph

0040 through page 3, paragraph 0046. Accordingly, no new subject matter is introduced by way of the new claims.

CONCLUSIONS

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-4, 21-24, 30, 32 and 37-38 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Applicant's undersigned attorney at the number indicated below.

Respectfully submitted,

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